PCB DFM Checklist

This checklist helps hardware engineers and engineering managers check a printed circuit board (PCB) for Design for Manufacture (DFM) and Design for Test (DFT) before releasing it for fabrication. It covers fabrication rules, components, assembly, testability and documentation, so issues that cause low yield, rework or a board respin are found while they are still cheap to fix.

Technically reviewed by the EmbedCrest engineering team Updated November 16, 2026

How to use this checklist

Run the checklist before every release of production intent layout, together with the fabricator and assembler capability documents. Note the rule or capability each item is checked against. Discuss any item that needs an exception with the manufacturer and record the agreed outcome in the release notes.

Fabrication

- [ ] Do trace width, spacing and annular ring meet the chosen fabricator's stated capability with margin?
- [ ] Is the layer stack up, material and copper weight agreed with the fabricator?
- [ ] Are controlled impedance traces specified with target values and tolerances?
- [ ] Are via types, drill sizes and aspect ratios within the fabricator's standard process?
- [ ] Is copper balanced across layers to limit board warpage?
- [ ] Are board outline, cut outs and mounting holes dimensioned in the fabrication drawing?

Components and bill of materials (BOM)

- [ ] Does every footprint match the manufacturer recommended land pattern for the exact part number?
- [ ] Are critical components checked for lifecycle status and lead time before release?
- [ ] Does each critical part have at least one approved alternate with a compatible footprint?
- [ ] Are moisture sensitive components identified for handling during assembly?
- [ ] Are component values, tolerances and voltage ratings checked against worst case conditions?

Assembly

- [ ] Are fiducials placed on the board and on the panel for pick and place alignment?
- [ ] Is component spacing sufficient for placement, inspection and rework?
- [ ] Are polarity and pin 1 markings clear on the silkscreen for every polarised part?
- [ ] Is the panelisation method, tabs or V score, agreed with the assembler?
- [ ] Are heavy or tall components placed to avoid shadowing during soldering?
- [ ] Is through hole component soldering method defined, such as wave, selective or hand?

Testability

- [ ] Are test points available on power rails, critical signals and communication buses?
- [ ] Is test point spacing compatible with flying probe or bed of nails fixtures?
- [ ] Is a programming and debug interface accessible on the assembled board?
- [ ] Is a functional production test defined with pass and fail limits?
- [ ] Can each board be identified by a serial number or label for traceability?

Release package

- [ ] Are Gerber or ODB++ files generated from the released revision and checked in a viewer?
- [ ] Is the BOM exported with manufacturer part numbers, quantities and reference designators?
- [ ] Are pick and place files, assembly drawings and fabrication notes included?
- [ ] Is the board revision marked on the copper or silkscreen?
- [ ] Is the release package stored under version control with a matching tag?